

A state machine, a counter, and related method for gating redundant triggering clocks according to the initial states is provided. The state machine includes a plurality of state units and a clock gating circuit. Each of the state unit is triggered by a clock to generate a corresponding varying state, and the clock gating circuit is capable of selectively withholding a triggering clock to at least one state unit according only to an initial state, such that the selected state unit(s) will not be triggered by the triggering clock while the rest of the state units are triggered by the triggering clock to update their corresponding states.

## Figures